All Digital Low Power DLL Based Frequency Multiplier Design by using 0.35-μm Process CMOS Technology

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Abstract—This paper shows the chip level implementation of an all digital low power DLL (Delay Locked Loop) based frequency multiplier. Due to all digital components it consumes very low power. To incorporate the digital configuration the charge pump was replaced by a counter. The total system consists of a phase detector, an up/down counter, the delay line, clock divider, and the frequency multiplier. In this paper the frequency multiplying technique is performed by using an edge combiner based clock synthesis system, which is implemented by C2MOS logic. The whole system was initially verified by simulation and later on was sent for fabrication on a chip. The fabricated chip has been tested, measured and compared with the simulated results. The reference clock frequency is 250 MHz and the output is a multiplied clock frequency of 1 GHz and multiplication factor is 4. The measured power consumption of the chip was 219 mW.

Index Terms—C2MOS, Delay Line, Delay Locked Loop, Frequency Multiplier, Clock Divider.

I. INTRODUCTION

The modern VLSI circuit society is developing day by day and to cope with that on chip high speed frequency multiplier is needed. One predictable way of multiplication is PLL (Phase Locked Loop); however it is a higher order system with stability issue. A critical part of a PLL is the loop oscillator which is highly sensitive to power supply noise, process variations, and operating conditions. On the other hand delay locked loop based frequency multipliers with first-order loops [1] have been anticipated with more strong constant performance. A DLL offers better jitter performance than a PLL, so it is more suitable for practical applications [1]-[4].

The proposed architecture has the phase detector subsystem generates an up/down signal based on the phase difference between reference clock and the delayed version of the clock from the Bit controlled Delay line block. The up/down counter subsystem counts either up or down based on the signal from the phase detector. The low frequency clock to the counter subsystem is generated by the clock divider subsystem. The clock divider subsystem generates a clock frequency of (Reference Clock frequency/4). The output of the counter controls the load (capacitors) of the delay elements in the delay line. The counter continues to alter the delay line until the delay line produces a delay of 1 clock period. The delay line consists of 8 stages which produces 8 different phases of the reference clock input. The phases are 45, 90, 135, 180, 225, 270, 315 and 360 degrees respectively. Each of these output in turn connected to the frequency multiplier which generates an output of 4 times the reference clock. The verification interface at the test chip refers to the pin outs which are provided for debugging and testing purposes on chip. The nodes for testing of Phase detector (PD), counter (b0 (LSB of counter)) and delay line (delayed) are taken as the output pins through the output buffers. These will be utilized during the testing of the chip after the manufacturing process. The reference clock frequency is 250 MHz and the output is a multiplied clock frequency of 1 GHz.

II. FREQUENCY MULTIPLICATION

The below figure shows two multiplier and both can be used for high frequency multiplication. In Fig. 1 (a) PLL-based structure is shown where output frequency is divided by a factor M before comparing the reference clock in PFD (phase frequency detector). In Fig. 1 (b) an all digital DLL-based structure is shown.

Fig. 1. Frequency multiplication (a) PLL-based and (b) DLL-based.

To describe Fig. 1 the frequency of the reference clock is compared with the Bit controlled Delay line delayed version
clock that is generated with an initial Bit controlled Delay line settings. Depending on the phase difference between two clocks, UP or DOWN output signal of the phase detector (PD) is activated. Counter subsystem increments or decrements the control bits based on the UP or DOWN signal received from PD. The counter value represents the control bits to the Bit controlled Delay line, which generates 8 equidistant phases of the reference clock. The delay of these signals is proportional to current counter value. Then the eighth clock signal is compared with the reference clock and a new UP or DOWN signal is generated depending on the phase difference. This feedback procedure is repeated until the DLL is locked. At locked state the PD oscillates between UP and DOWN.

By comparing these two structures it can be seen that for rational number multiplication by $M/N$ in the PLL, the VCO and the dividers operate at $N$ times higher frequency than the actual needed frequency which increases power consumption and the dividers also add parasitic to the output of the VCO.

No let consider the transfer function of the PLL and DLL in general. The closed loop transfer function of PLL is

$$H(s) = \frac{K_{cp}K_{vco}(R_pC_p + 1)}{s^2 + K_{cp}K_{vco}R_pC_p + K_{cp}K_{vco}}$$

(1)

where $K_{vco}$ is the gain of the VCO and $K_{cp}$ for a charge-pump current of $I_p$ is defined as [3]

$$K_{cp} = \frac{I_p}{2\pi C_p}$$

(2)

On the other hand the closed-loop transfer function of the DLL is $K_{dl}$ [3]

$$H(s) = \frac{K_{cp}K_{vcdl}}{s + K_{cp}K_{vcdl}}$$

(3)

Where $K_{vcdl}$ is the gain of the delay lines and $K_{cp}$ is described in (2). From (1) and (3), it is clear that PLL is a second order system where DLL is a first order system with confirmed stability. The difference between these two systems is the VCO inside the loop which adds an extra pole to the system. In the next section the description of all the subsystem circuit along with the layout of those will be given [3].

III. FREQUENCY MULTIPLIER SUB-SYSTEM DESCRIPTION

A. Clock Divider

The clock divider subsystem generates a low frequency clock required by the counter subsystem. The clock divider subsystem takes reference clock as the input and generates a output clock of frequency equal to reference clock/4. It consists of two T-flip-flops connected in series to achieve the required clock frequency. Fig. 2 below shows the waveform of the clock divider.

![Fig. 2. Clock Divider waveform.](image)

B. Phase Detector

The phase detector is used to acquire the phase relationship between the reference clock input and its delayed version from the delay line. The phase detector is used to provide phase discrimination and generate a control signal which is then used to speed up or slow down the reference clock in delay line, so that a desired relationship of one clock period between the reference clock and the delayed version is obtained. Fig. 3. below shows schematic and layout diagram of the PD respectively.

![Fig. 3. Phase Detector (a) Schematic Diagram and (b) Layout.](image)
C. Up-Down Counter

When the delayed version of clock is less than one clock period of reference clock the phase detector generates an up signal to the counter and the counter will count up. The out of the counter will act as a control bits to the delay line which cause the delay line to increase its delay in order of delay steps. On the other hand when delayed version of the clock is delayed by more than one clock period the phase detector generates a down signal which will make the counter count down. As a result it will make the delay line to decrease its delayed step. Fig. 4. below shows layout and waveform of the counter respectively.

D. Bit Controlled Delay Line

The clock input of 250 MHZ is delayed by Bit controlled Delay line in number of steps. The delay line is constructed from symmetrical delay elements. It is composed of 8 delay elements in order to produce 8 phases to the multiplier. The delay element is digitally controlled by the control bits from the counter. The delay is varied in steps by switching various values of capacitors to the constant current source. The delay is related to the capacitance by the equation given below. The relationship between the current, capacitor, voltage and time is given by the formula

\[ I = \frac{cv}{t} \]

(4)

\[ I = \frac{\mu Cox}{2} \left( \frac{W}{L} \right) (Vgs - Vt)^2 \]

(5)

Each delay element comprises five stages of capacitors which can produce '32' delay steps at 100ps each. The transmission gate is used as the switch to connect the capacitors to the constant current source. Every delay element produces 180 degrees DC phase shift and an AC phase shift of 45 degrees at locked condition. The figure below shows the Bit controlled delay lines and delay elements.

![Fig. 5. Bit Controlled (a) Delay Line and (b) Delay Elements.](image)

The delay element is controlled individually by the control bits from the counter. As shown in the figure, the total capacitance and the transmission gate size at each stage is increased progressively. N-MOSFET is used; its gate capacitance acts as the capacitor. By varying the width of the MOSFET a range of capacitance can be achieved. In order to make the delay steps in linear, the size of the transmission gate at each stage has been increased. The output inverters connected after the capacitors are for producing the minimum delay to avoid “false-locking” in DLL.

This delay line achieves a minimum of 3ns to the maximum of 5.4ns delay in steps of approximately 100ps as shown in the plot given below.
These are the layouts of delay line and delay element below.

The power consumption of the Delay line running at counter steps from 0 to 31 is measured to 14 mw in layout level and 12 mw in schematic level at the supply voltage of 3.3v. The rise time of the pulse output in layout is measured to 446ps.

E. C2MOS Frequency Multiplier

To multiply with N, the architecture needs 2N input clocks. The operation of the proposed multiplier is as follows.

Every multiplier stage is composed of P-type and N-type C2MOS inverter. 2N output clocks of Bit controlled Delay line are fed to the multiplier. Suppose that the signals Clki are Bit controlled Delay line output clocks and tinv is the propagation delay of each CMOS inverter.
During falling edge of Clki which is fed to the PMOS transistor, both PMOS transistors are turned on for 5tinv, and the output will go high. Then as Clki+1 arrives Tp/2N second later than Clki, the output will go low in the rising edge of Clki+1. In order to drive the large capacitive load of the multiplier circuit, a buffer is used after Bit controlled Delay line. Multiplication factor, N, depends on the number of Bit controlled Delay line outputs and cascaded stages. In this project it employs 4 cascade stages of multiplier circuit to implement multiplication by 4.

From the above waveform it can be seen that eight clocks are delayed such that the phase difference between them equals 1/8 reference clock period. These clocks are generated by Bit controlled Delay line. In phase locking state, these clocks are the outputs of the Bit controlled Delay line stages.

IV. MEASUREMENT RESULTS
A test chip has been designed in 350-nm CMOS process. In the chip the verification interface provides the accessibility to the important nodes of Delay locked loop for high speed testing after its chip manufacturing. The verification interface has the pin outs, which are provided for debugging and testing purposes on chip, to the internal nodes of the chip. The nodes taken as the test points are Phase detector output (PD), counters LSB bit (b0) and delay line (f-delayed). These are taken as the output pins through the output buffers. These buffers enable the connection to the outside worlds.

The PCB along with the chip is connected to the signal generator, DC power supply, oscilloscope, multi-meters and spectrum analyzer in the following block diagram. Once the stated configuration of the testing circuit is setup, then the DC power supply and the clock signal voltage with some low values are applied, but the output did not come. To get the output inputs are kept increasing and finally when it got its desired input the output appeared. The various inputs that have been applied and the corresponding outputs are given in the following table.

<table>
<thead>
<tr>
<th>S/N</th>
<th>VDD</th>
<th>VPP</th>
<th>Current</th>
<th>fIN</th>
<th>fOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1v</td>
<td>1v</td>
<td>20mA</td>
<td>100MHz</td>
<td>--</td>
</tr>
<tr>
<td>2</td>
<td>2v</td>
<td>2v</td>
<td>31mA</td>
<td>200MHz</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>3.23v</td>
<td>3.04v</td>
<td>68mA</td>
<td>250MHz</td>
<td>1.0003GHz</td>
</tr>
</tbody>
</table>

The following pictures show the output signal along with the input signal.
TABLE II: THE CHARACTERISTICS OF THE FREQUENCY MULTIPLIER

<table>
<thead>
<tr>
<th>Power consumption of the circuit</th>
<th>219mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption of the chip</td>
<td>161mW</td>
</tr>
<tr>
<td>Output Frequency</td>
<td>1,000GHz</td>
</tr>
<tr>
<td>Input Frequency</td>
<td>250MHz</td>
</tr>
<tr>
<td>Multiplication Factor</td>
<td>4</td>
</tr>
<tr>
<td>Input Frequency lock range</td>
<td>190MHz-320MHz</td>
</tr>
</tbody>
</table>

TABLE III: PERFORMANCE COMPARISON BETWEEN SIMULATION AND MEASURED RESULT FROM THE CHIP

<table>
<thead>
<tr>
<th>Simulated power consumption (Chip)</th>
<th>161mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured power consumption (Chip)</td>
<td>219mW</td>
</tr>
<tr>
<td>Simulated output frequency</td>
<td>1GHz</td>
</tr>
<tr>
<td>Measured output frequency (Chip)</td>
<td>1,000GHz</td>
</tr>
<tr>
<td>Simulated duty cycle of the output</td>
<td>56.00%</td>
</tr>
<tr>
<td>Measured duty cycle of the output (Chip)</td>
<td>60.00%</td>
</tr>
<tr>
<td>Simulated multiplication factor</td>
<td>4</td>
</tr>
<tr>
<td>Measured multiplication factor (Chip)</td>
<td>4</td>
</tr>
<tr>
<td>Simulated input frequency locking range</td>
<td>185MHz-333MHz</td>
</tr>
<tr>
<td>Measured input frequency locking range (Chip)</td>
<td>190MHz-320MHz</td>
</tr>
</tbody>
</table>

V. CONCLUSION

An achievement of all digital Delay Locked Loop based frequency multiplier in 0.35-µm CMOS has been obtained. In this architecture there is no part of PLL is used instead of that counter and clock divider is introduced to the structure. Compared to other design it is clearly visible that this structure is consumes less power than others if it is in the same process. In the next phase the design will be done in 65-nm CMOS process.

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REFERENCES