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Design of an extremely low power FIR filter for sensors at 45nm process using source-coupled logic in sub threshold region and leakage current reduction technique

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***Abstract*— The performance of source-coupled logic at sub threshold region for ultra-low power applications is remarkable. It shows that the power consumption of these circuits can be reduced well below the sub threshold leakage current of static CMOS circuits. Where the leakage current constitutes a significant part of the power dissipation STSCL circuits exhibit a better power-delay performance compared to their static CMOS gates. Also for sensor systems, such as large-scale distributed smart dust sensors, digital filters are common components. So less power consumption is a prior choice. With the transistor technology scaling becoming more and more sensitive to gate leakage, it has become a necessity to find ways to minimize the flow of leakage current. The STSCL style is in this paper used to design a digital filter, applicable for the audio interface of a smart dust sensor where the sample frequency will be 44.1 kHz. The power consumption is calculated along with the delay in order to present the power delay product (PDP) such that the performance of the sub-threshold logic can be compared with corresponding CMOS implementation. The simulated results shows a significant reduction in energy consumption (in terms of PDP) with the system running at a supply voltage as low as 0.2 V using STSCL.**

***Index Terms*— STSCL, CMOS, PDP, CSD Multiplier, FIR Filter.**

I. INTRODUCTION

To minimize the power consumption in a digital circuit, source-coupled logic in sub threshold region is very unique. In ultra-low power applications, where the power dissipation is a crucial parameter, supply voltage is generally reduced below the threshold voltage of MOS devices [5]. Reducing the supply voltage or choosing high threshold voltage (HVT) devices results in a smaller V_T value and hence less power consumption [2]. Wide variation of circuit characteristics, such as speed of operation and power dissipation, due to variations of process parameters, supply voltage, and temperature (PVT) is the other important issue in the design of ultra-low power digital circuits in modern nanometer scale technologies [6]. The effects of such variations become more evident when the devices are biased in sub threshold regime. The precise control on the power consumption of each gate makes this topology very suitable for very low bias current operations where the dissipation of conventional static CMOS circuits is limited by their sub threshold leakage current. The performance variation due to the PVT variations is also much less in this type of circuits compared to the static CMOS topology. In this article, an analytical approach for analyzing and comparing the leakage and power-delay performance of CMOS and STSCL topologies will be presented. Also a digital filter has been designed for Smart sensor's to compare the power consumption, as it is one of the key components of the DSP section which is required for eliminating any unwanted signals or noise. It is important for the longevity of these sensors that they should consume as low power/energy during application (without degrading performance by too much) and have a long lasting battery life. For achieving such longevity in respect to battery life, the digital sections of these sensors need to be run under lower supply and also dissipate as low leakage as possible. But it has to be kept in mind system performance or delay must not be harmed by great amount in the course of reducing supply voltage. For current MOSFET processes at channel lengths below 65 nm the leakage currents and its impact on performance has become a factor of concern. At a 45 nm node, or below, the trend is that the leakage current continues to have a negative impact on performance as well as the energy consumption [20]. The usage of dynamic voltage scaling can reduce the dynamic energy dissipation, but quite often this also increase the leakage current. Further on, in 45 nm or lower the gate-to-channel tunneling effects is a large contributor to the overall energy consumption. Leakage current can also consist of sub threshold leakage, which is significant during the off-state operation mode. In CMOS the sub threshold leakage can be reduced by using MOSFET devices with high threshold value which in turn narrows down the possible range for voltage scaling. Further on, reducing supply voltage in attempt to reduce power consumption has a drawback as it increases the propagation delay. So even though power consumption is less but due to larger delay, the energy consumption of the system increases, hence performance as well as battery life for the system degrades. The mentioned drawbacks can be solved using several different techniques like power gating [1] or multi-threshold CMOS libraries [2]. In some sense, this increases the design complexity and imposes difficulties for the verification and verification tools. For example, we might have to introduce several different clock domains and power

modes/domains to maintain the system performance under all conditions. Sub-threshold source coupled logic (STSCL) is a fairly new kind of logic style that have recently came into consideration for its ability to operate and perform at sub-threshold region ($V_{in} < V_t$) of a MOSFET device [3]. This operating ability at sub threshold or linear region allows the use of gates implemented with STSCL and they can be operated at very low supply voltage without little harm on system performance. Thus providing a low energy consumption rate for a system implemented with STSCL gates. The understandings of the STSCL topology is applied to a fifth-order FIR transposed direct form filter. We are aware that FIR filters might require more computational power, but as we are focusing on observing the advantages of using STSCL topology over CMOS in terms of energy consumption, this type of filter architecture is better suited for serving the purpose. The basic STSCL inverter circuit and the required bias circuit for operating the logic at sub-threshold region have already been designed and tested in other research papers [1]. Thereby focus in this specific paper is given on the STSCL implemented gates needed for filter designing, and the minimal configuration at which the gates can operate suitably. In Section II and III insights on the implementation of the STSCL based gates, the amplifier needed for the replica bias circuit and the 5th order filter in STSCL gates. Finally the paper concludes with the comparison of their performance with CMOS gate implementation.

II. Basic Logic Gates in STSCL

The Exclusive or (XOR/XNOR), or (OR/NOR), and (AND/NAND) gates, along with flip-flops (DFF/DNFF) are the most commonly required logic gates to design a digital filter that will be applicable to smart dust sensor modules implementation. The logic gates are designed to perform under sub-threshold region at scaled down supply voltages; down to 0.2 V. The provided bias currents per stage are in the order of 250 pA. The PMOS (acting as high resistive load [21]) widths are 135 nm (has to be low in order to achieve a high load resistive value, this is mandatory for running the gates at sub-threshold region) and the NMOS input devices are off widths 675 as they need to have stronger driving capability to perform full logic swing of the next logic stages.. The circuit schematics for the XOR, OR, AND gates and DFF are given in Figure 1. The results of performed simulations on XOR, OR and AND given in TABLE 1. The simulations are performed with inputs at a rate of 10 kHz. For the DFF a clock frequency of 44.1 kHz is applied with the input data rate at 10 kHz, like before, and an output duty factor of 50 % [20].

TABLE I: Power-Delay table for STSCL based gates

Logic	Temperature	Power [nW]	Delay [µs]
XOR/XNOR	-20	0.152	2.52
	70	1.11	0.096
OR/NOR	-20	0.157	1.489
	70	1.15	0.129
AND/NAND	-20	0.15	1.422
	70	1.15	0.135
DFF	-20	0.442	2.97
	70	3.366	0.152

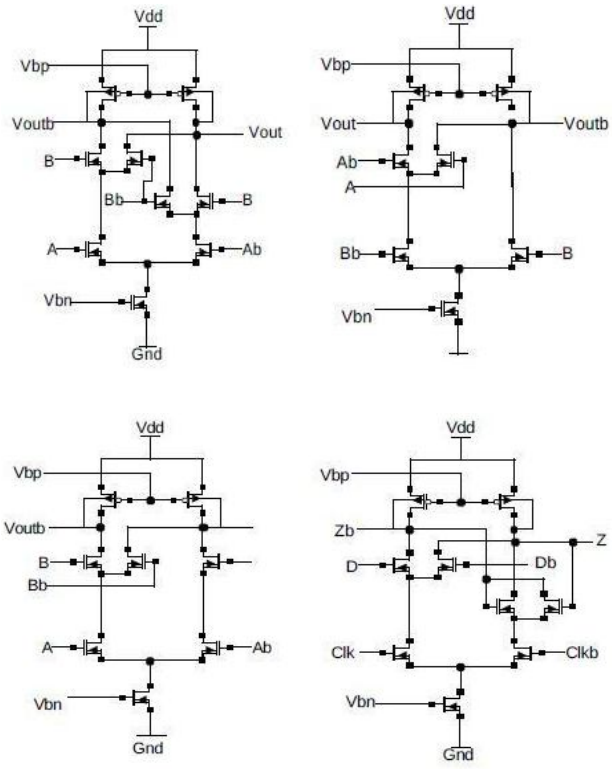

Fig. 1. XOR/XNOR, OR/NOR, AND/NAND, DFF.

Folded-cascode architecture has been used to design the amplifier required for the design of replica bias circuit. In Figure 2 shows a schematic view of the amplifier with modified PMOS load device [21]. Similar PMOS load devices have been used for the design of the amplifier's architecture in order to operate it at sub-threshold region. Even-though this architecture uses more number of transistors but it can easily be applicable to operate at very low voltage. Other architectures like two-stage OTA can also be used which require less number of transistors but is difficult to be operated at sub-threshold regime [20].

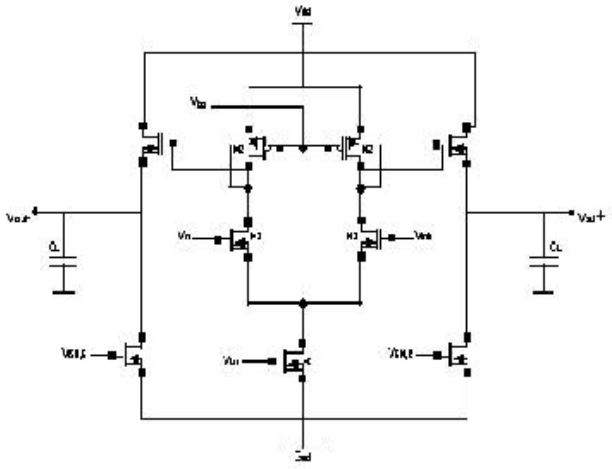

Fig. 2. Folded-cascode amplifier (operates in sub-threshold region).

III. STSCL BASED FIR FILTER

The fifth order FIR filter designed in this paper is a conventional, widely-used and foremost verified structure (as in Figure 3). IIR filter can be also used instead of the FIR filter but IIR filters have more design complications compare to FIR filter. The filter has a of serial-input and serial-output form with a sampling frequency of 44.1 kHz, and for the multiplication with fixed coefficients a five-bit of serial/parallel multiplier [19] has been used. The response for the filter is given in Figure 4. The coefficients are represented in canonic signed digit (CSD) form. CSD is an optimized form compares to the more conventional two's complement form [21]. The CSD based S/P multiplier uses lesser hardware resources and hence lower the power down to further level.

The supply voltage is 0.2 V with a bias current at 250 pA per stage as discussed before. The supply voltage of 0.2 V is the limit up to which the system can be operated. The basic tryout for the different supplies allowed seeing how well a system could perform under critical situation while STSCL gates have been configured to run at their minimum operating specification. Simulations have been operated and compiled on Cadence Virtuoso v6.14, using both CMOS and STSCL at -20°C and 70°C temperature. The results of the PDP along with the delay for the fifth-order filter are shown in TABLE 2 [20].

TABLE II: PDP VALUES FOR STSCL AND CMOS BASE FIFTH-ORDER FIR FILTER

Logic	STSCL		CMOS	
Temp [^{O}C]	-20 ^{O}C	70 ^{O}C	-20 ^{O}C	70 ^{O}C
PDP [fJ]	600.4	45.81	784.6	46.23
Delay [µs]	3.25	1.06	5.65	0.67

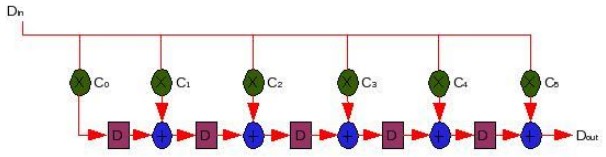

Fig. 3. Fifth-order FIR Filter

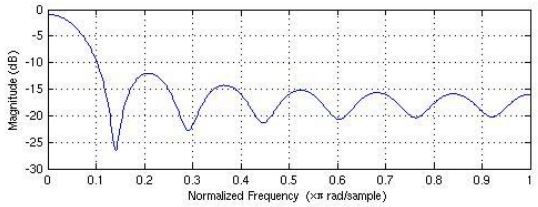

Fig. 4. Response Fifth-order FIR Filter

IV. PERFORMANCE COMPARISON

Before designing the finite impulse response length (FIR) filter using STSCL, a 4-by-4 array multiplier is designed in order to test and verify the significance of using STSCL over CMOS. The multiplier chosen has a tree-based structure and the block diagram is shown in Figure 4. The structure was designed in STSCL at a 0.2-V supply voltage with a 250 pA bias current per stage. In CMOS we had to use a supply voltage of 0.5 V to guarantee operation using the standard cells at hand. The circuit operated at -20^{o} C. The simulated power delay product (PDP) turned out to be comparatively smaller for STSCL than CMOS.

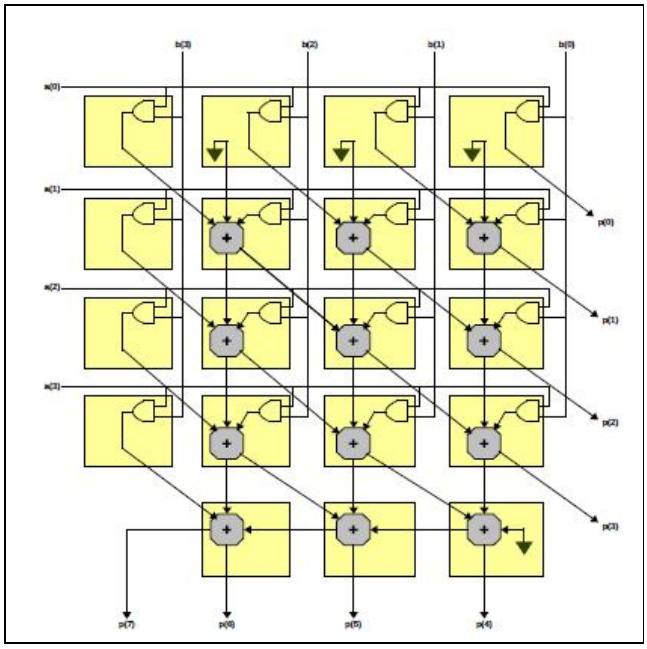

Fig. 5. Block diagram of a 4-by-4 array multiplier.

Another important parameter is the additional chip area which the STSCL will occupy compared to conventional CMOS. An estimated area was obtained from the layout of the 4-by-4 multiplier designed in two different logic styles (STSCL and standard-cell CMOS) and the results are shown in TABLE II Even though area is some three times larger for STSCL it should be mentioned that the area estimation is considered using quite a few bias circuits rather than a single bias circuit for the whole multiplier. Also the delay for the STSCL is more than 35% longer compared to CMOS but the power delay product is lower. The results show that the overall energy consumption for a 4-by-4 multiplier is less using STSCL than CMOS.

TABLE III: PERFORMANCE COMPARISON FOR 4 BY 4 MULTIPLIER

Logic	STSCL	CMOS
PDP [fJ]	302.4	313.15
Delay [µs]	52.47	38.65
Area [µm^2]	330	100

V. CONCLUSION

The performance for STSCL at extreme condition is comparatively better than CMOS in a 45 nm process at a supply voltage of 0.2 V. The most important factor found in the simulations is that the energy consumption for STSCL is less than CMOS which suggests trying out further implementation of all the digital components of the sensor in STSCL. The STSCL topology provides a more flexible design option for ultra-low-power applications. The frequency range, in which STSCL topology exhibits a superior performance over static CMOS topology, depends on the logic depth and also the leakage current in CMOS circuits.

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